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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,544	04/12/2004	Peter Pfann	P2003,0235	1800

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EXAMINER	
JACKSON, BLANE J	
ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,544	PFANN ET AL.	
	Examiner	Art Unit	
	Blane J. Jackson	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-19, 21-23* is/are rejected.

7)☒ Claim(s) *13 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 14-19 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vu et al. (US 6,002,926) in view of Auvray (US 5,953,641) and Horton et al. (US 6,424,826).

As to claim 1, Vu teaches an integrated transceiver circuit (figure 1, column 5, line 15 to column 6, line 49, transceiver formed on a single semiconductor body or chip (51)) comprising:

A reception path including a mixer unit for demodulating a received signal and also including an analog/digital converter unit connected downstream from the mixer unit (figure 1, column 6, lines 9 to column 8, line 44, downconverter (42) and column 11, line 35-51, ADC (52)), and

A first voltage controlled oscillator (column 8, line 45 to column 9, line 19, PLL or receiver channel selector (46) with VCO (76)).

Vu teaches an integrated radio frequency transceiver but does not teach it includes a first frequency divider connected between the first VCO and the mixer unit for obtaining a demodulating frequency for use by the mixer unit.

Auvray teaches a multimode radio frequency direct conversion quadrature transceiver comprising a first frequency divider connected between the first voltage controlled oscillator and the mixer unit for obtaining a demodulation frequency for use by the mixer unit, figure 1, column 4, lines 24-65, receiver mixers (MRI and MRQ), frequency divider (DIV)).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the frequency generation circuits of VU with the synthesizer/ divider circuit in the transceiver circuit of Auvray for multimode radio communication.

Vu modified does not teach a second frequency divider connected between the first voltage controlled oscillator and the analog/digital converter unit for obtaining a sampling frequency for use by the analog/digital converter unit.

Horton teaches a wireless mobile terminal including a global positioning system receiver wherein the GPS receiver comprises a second frequency divider (236) connected between the output of a first VCO (198) and the analog/digital converter unit in the GPS processor (214) for obtaining a sampling frequency for use by the analog/digital converter unit, figures 8 and 15, column 9, line 65 to column 10, line 7.

Since Horton also teaches a first frequency divider (240) connected between the first VCO and the mixer unit (242) for obtaining a demodulation frequency for use by the mixer unit, it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Vu modified with the additional frequency division approach of Horton to further configure a transceiver system for multimode/ multiband operation.

As to claim 2, Vu teaches the integrated transceiver circuit of claim 1 further including a transmission path having a modulator for modulating a signal to be transmitted a second voltage controlled oscillator (transmit channel frequency selector (24)) but does not teach third frequency divider connected between the voltage controlled oscillator and the modulator for obtaining a modulation frequency for use by the modulator.

Auvray teaches a transceiver comprising a single PLL (SYN) and single frequency divider (DIV) connected between the frequency synthesizer (SYN) or VCO and demodulation/ modulation circuits for selective use by the reception and transmission path, figure 1. Consequently, since Auvray teaches the idea of selective use of frequency division to the reception and transmit signal paths for the purpose of multimode operation, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the dual VCO system of Vu of Vu modified to include a frequency divider as taught by Auvray but for both VCO circuits as taught by Vu for multimode operation of the transceiver.

As to claim 14 with respect to claim 2, Vu of Vu modified teaches the reception path includes a digital signal processing unit connected downstream from the analog/digital converter unit, the digital signal processing unit having an output which forms a digital output of the reception path (figure 1, column 6, lines 23-49, DSP (50) includes the demodulation function of the reception path which is shown with ADC (52) on the front end).

As to claim 15 with respect to claim 14, Vu of Vu modified teaches wherein the reception path is not disclosed after the demodulator/DSP (50), figure 1, and is silent as the reception path includes a digital/analog converter unit coupled to the output of the DSP unit, the digital/analog converter unit having an output which forms an analog output of the reception path.

Auvray teaches a multimode direct conversion digital transceiver where the reception path comprises a codec coupled to the demodulation stage which includes the digital to analog function to drive the voice speaker (HP) and analog to digital function for voice microphone (M) input, figure 1, column 2, lines 35-67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to alternatively complete the reception circuit of Vu in the application of Auvray for voice communications.

As to claim 16 with respect to claim 2, Vu of Vu modified teaches the integrated transceiver circuit including a second phase locked loop connected between the reference frequency input and the second voltage controlled oscillator (figure 1, column 5, line 48 to column 6, line 5, line 45 to column 9, line 20, local oscillator (30) produces the frequency reference which is coupled to the transmit channel frequency selector (24) or PLL comprising the second VCO (38)).

As to claims 17 and 18 with respect to claims 16 and 2, Vu of Vu modified teaches the integrated transceiver circuit including a reference frequency input for

receiving an external reference frequency and a first phase locked loop connected between the reference frequency input and the first voltage controlled oscillator (figure 1, column 8, line 45 to column 9, line 20, local oscillator (30) produces the frequency reference which is coupled to the receiver channel selector (46) comprising the first VCO (76)).

As to claim 19, Auvray of Vu modified teaches the modulator is an IQ modulator (figure 1, column 2, line 61 to column 3, line 8).

As to claim 21, Vu of Vu modified teaches the integrated transceiver of claim 1 wherein the reception path includes a low-pas filter unit connected between the mixer unit and the analog/digital converter unit (figure 1, column 6, lines 9-13, LPF (45)).

As to claim 22 with respect to claim 1, Vu teaches a downconverter, column 6, line 52 to column 7, line 25, but does not teach the mixer unit is an IQ mixer.

Auvray teaches a multimode transceiver utilizing a quadrature reception mixer and transmit modulator, figure 1, column 2, line 61 to column 3, line 24.

It would have been obvious to one of ordinary skill in the art at the time of the invention to recognize the conversion stages of Vu are alternatively configured in quadrature as taught by Auvray in accordance with well known design techniques in multimode transceivers.

As to claim 23 with respect to claim 1, Auvray of Vu modified teaches the first and second frequency dividers are integer dividers (figure 1, column 4, lines 25-48, DIV is a switchable frequency changer where the division example is the integer 2).

Claims 3-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vu et al. (US 6,002,926), Auvray (US 5,953,641) and Horton et al. (US 6,424,826) and further in view of Khlat (US 7,039,438).

As to claim 3 with respect to claim 2, Vu modified teaches *the reception path* includes an analog/digital converter unit connected downstream of the modulator including a frequency divider connected between the first VCO and the analog to digital converter *but Vu of Vu modified does not teach the transmission path* includes a digital/analog converter unit connected upstream of the modulator and including a fourth frequency divider connected between the second VCO and the digital/analog converter unit for obtaining a sampling frequency for use by the digital/analog converter unit, column 5, lines 15-47.

Khlat teaches a multimode transceiver comprising a transmission path (figure 3) that includes a digital/analog converter unit connected upstream of the quadrature modulator, including a frequency divider (dividers/switch with output fovs-TX) connected between the reference PLL and the digital/analog converter unit for obtaining a sampling frequency for use by the digital/analog converter unit.

It would have been obvious to one of ordinary skill in the art at the time of the invention recognize the transceiver system of Vu modified would require the DAC and

sampling frequency divider architecture as disclosed by Khlat to support multiband/ multimode operation.

As to claim 4, Vu of Vu modified teaches the integrated transceiver circuit of claim 3 including a reference frequency input for receiving an external reference frequency and a first phase locked loop connected between the reference frequency input and the first voltage controlled oscillator (figure 1, column 8, line 45 to column 9, line 20, local oscillator (30) produces the frequency reference which is coupled to the receiver channel selector (46) comprising the first VCO (76)).

As to claims 5 and 12 with respect to claims 4 and 3, Vu of Vu modified teaches the integrated transceiver circuit including a second phase locked loop connected between the reference frequency input and the second voltage controlled oscillator (figure 1, column 5, line 48 to column 6, line 5, line 45 to column 9, line 20, local oscillator (30) produces the frequency reference which is coupled to the transmit channel frequency selector (24) or PLL comprising the second VCO (38)).

As to claims 6, 8 and 10 with respect to claims 5, 4 and 3, Vu of Vu modified teaches the reception path includes a digital signal processing unit connected downstream from the analog/digital converter unit, the digital signal processing unit having an output which forms a digital output of the reception path (figure 1, column 6,

lines 23-49, DSP (50) includes the demodulation function of the reception path which is shown with ADC (52) on the front end).

As to claims 7, 9 and 11 with respect to claims 6, 8, and 10, Vu of Vu modified teaches wherein the reception path is not disclosed after the demodulator/DSP (50), figure 1, and is silent as the reception path includes a digital/analog converter unit coupled to the output of the DSP unit, the digital/analog converter unit having an output which forms an analog output of the reception path.

Auvray teaches a multimode direct conversion digital transceiver where the reception path comprises a codec coupled to the demodulation stage which includes the digital to analog function to drive the voice speaker (HP) and analog to digital function for voice microphone (M) input, figure 1, column 2, lines 35-67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to alternatively complete the reception circuit of Vu in the application of Auvray for voice communications.

Allowable Subject Matter

Claims 13 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon but considered pertinent to applicant's disclosure includes: Vogt et al. (US 5,430,890), Li et al. (US 6,415,001), Lee et al. (US 2003/0118135), Warren et al. (US 6,690,313), Clement et al. (US 6,856,266), Tso et al. (US 6,856,794) and Olip (US 7,003,274).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Friday, 9:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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